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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,260	06/26/2002	Katsuyuki Sakuma	JP920010143US1	2088

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IBM CORPORATION, T.J. WATSON RESEARCH CENTER
P.O. BOX 218
YORKTOWN HEIGHTS, NY 10598

EXAMINER	
DINH, DUC Q	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,260	SAKUMA ET AL.	
	Examiner	Art Unit	
	DUC Q DINH	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *8,9,13,14,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,10-12 and 15,17-20* is/are rejected.

7)☒ Claim(s) *3 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claim 1-7, 10-12 and 15-20) in the reply filed on August 13, 2004 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 6-7, 10-12 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu (U. S. Patent No. 5,801,674).

In reference to claim 1 Shimizu discloses a Liquid Crystal Display in Fig. 1-3 comprising: liquid crystal panel 1 for forming an image display area, a driver ICs 3-6 for applying a voltage to the panel, a controller 7 for processing signal received from host's side and supplies process signals to the driver ICs (Fig. 1). In addition, Fig. 2-3 show a single driver IC with the input circuit 11 having delay circuit for delaying the start timing for writing data to the panel as claimed. (col. 4, lines 22-55)

In reference to claim 4, Shimizu discloses a Controller 7 outputs clock signal supplied to the drivers 3-6, a sync containing a start signal to the driver ICs 3-6 indicating the delay time for the input circuit 1 in driver IC as claimed. (col. 52-65).

In reference to claims 6-7, Shimizu disclose the data fetch starting signal and load signal which the sequence control circuit 13 outputs to control the data register 15 and output latch 16 are generated in the cascade connection control circuit 12 by decoding the SYNC signal. That is, the cascade connection control circuit 12 receives a clock signal CLOCK' supplied via a buffer 18, a common start signal (START') obtained by decoding the synchronization signal (SYNC') output from the input circuit 11, and an enable input E1 input from the EI terminal as inputs to create a start signal START for controlling the timing at which the data register 15 starts the data fetching operation and a load signal LOAD for controlling the timing at which the output latch 16 outputs display data to the LCD driving circuit 17 (col. 4, line 61- col.5, line 7).

In reference to claim 10, Shimizu discloses in Fig. 3, input circuit 11 having flip flops FF11 and delay circuits 112a-n, 114... (Corresponding to the setting register and counter) for storing information about writing delay timing for delaying writing time of the data to the panel; and sequence control circuit 13 for activating the delayed output start signal; and control circuit 17 for controlling the writing of the panel based on the output of the sequence control cirucuit 13 as claimed.

In reference to claim 11-12, refer to the rejection as applied to claim 4.

In reference to the method of claims 19-20, refer to the rejection as applied to the apparatus of claims 6-7.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2, is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (U. S. Patent No. 5,801,674) in view of Sasaki et al. (U. S. Patent No. 6,211,840), hereinafter Sasaki.

In reference to claim 2, Shimizu does not disclose that the driver ICs are mounted on the substrate of the display panel and power is supplied to the driver ICs via a physical wiring lines. Sasaki discloses in Fig. 1-2 and 11-13 a driver IC's for a Liquid Crystal Display is mounted on the substrate of the panel and power is supplied through wire lines as claimed.

It would have been obvious for one of ordinary skill in the art at the time of the invention was made to learn the teaching of Sasaki, i.e.: providing driver IC's on the display panel, in the device of Shimizu, in order to prevent an increase in the dimensions of the frame region and in the manufacturing cost (col. 2, lines 10-16).

6. Claims 5, 15, 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu in view of Hashimoto (U. S. Patent No. 6,628,259).

In reference to claim 5, Shimizu discloses everything except the LCD controller outputs serialized control data signal that include the polarity select signal indicative of polarity of the

liquid crystal output signal. Hashimoto discloses a controller for a multiple driver ICs for driving a source driver of a liquid crystal display output serialized control data signal that include POL signal as claimed (see Fig. 1).

It would have been obvious for one of ordinary skill in the art at the time of the invention was made to learn the teaching of Hashimoto, i.e.: providing the POL control signal from the controller, in the device of Shimizu, for improving the DC balance of the gray voltage provided to the display panel.

In reference to claims 15, 17, Shimizu discloses everything except means for outputting a control strobe signal to count the delay time stored in the driver ICs. Hashimoto discloses driver control circuit providing a strobe control signal for the driver ICs in Fig. 4.

It would have been obvious for one of ordinary skill in the art at the time of the invention was made to learn the teaching of Hashimoto, i.e.: provide the strobe control signal for the source driver ICs of Shimizu for controlling the timing at which the output latch 16 outputs display data to the LCD driving circuit 17.

In reference to claim 18, refer to the rejection as applied to claim 5.

Allowable Subject Matter

7. Claims 3 and 16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: none of the cited arts teaches or suggests

The liquid crystal display according to claim 1, wherein said driver applies a voltage to said Liquid crystal cells such that the driver lCs sequentially drive the liquid crystal cells starting from the downstream one located farthest away from a power source towards the upstream ones close to the power source (claim 3) or

The LCD controller according to claim 15, wherein said timing setting data output means outputs said timing setting data represents delay time to said liquid crystal cells starting from the downstream driver IC located farthest away from a power source. (claim 16)

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **DUC Q DINH** whose telephone number is **(703) 306-5412**. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD A HJERPE** can be reached on **(703) 305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivery response should be brought to: Crystal Park II, 2121 Crystal Drive, Arlington, Va Sixth Floor (Receptionist)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

DUC Q DINH
Examiner
Art Unit 2674

DQD
January 24, 2005

XIAO WU
PRIMARY EXAMINER